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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/028,276	02/24/98	ATSUMI S	17[illegible]

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EXAMINER	
FENTY, J	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/28/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/028,276	Atsumi
Examiner	**Group Art Unit**
Jesse A. Fenty	2815

☒ Responsive to communication(s) filed on *Apr 29, 1999*.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-9, 13, and 14* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-9, 13, and 14* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu et al. (U.S. Patent No. 4,471,373).

In re claim 1, Shimizu (Figs. 1-3, 18) discloses a semiconductor integrated circuit device comprising a semiconductor substrate (10) on which a plurality of transistors (Q1, Q2, QE1, QE2, QE3) including gate insulation films of different thicknesses are formed; an input/output terminal (5) formed on the substrate, a transistor (QE2) connected directly to the input/output terminal being one of the transistors other than a transistor having the thinnest gate insulation film.

In re claim 2, Shimizu discloses the device of claim 1, further comprising a power supply terminal (5), a transistor (QE3) connected directly to the power supply terminal being one of the transistors other than the transistor having the thinnest gate insulation film.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-9 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (U.S. Patent No. 4,471,373) as applied to claim 1 above.

In re claims 3-9 and 13-14, Shimizu (Figs. 1-3, 18) discloses the device of claim 1, including a memory array (2), a decoder portion (3), an input/output circuit (4), and enhancement type MIS transistors having a high breakdown voltage structure, i.e. a thick gate oxide film, and terminals for external connections (5) (column 1, lines 63-68; column 2, lines 23-63). Shimizu discloses the use of thin gate oxide transistors for the 'read' operation of an EPROM device and thick gate oxide transistors used for the 'write' operation, as well as other peripheral circuits (column 2, lines 45-51 Shimizu does not expressly disclose a ground terminal connected to the power supply terminal, a regulator circuit or a level shifter circuit of which one of the transistors receiving a lower level signal is a transistor having the thinnest gate insulation film. However, it would have been obvious to one skilled in the art at the time of the invention to couple a power supply line to a respective ground line. With the use of thin gate oxide transistors and lower voltages in the memory array and thick gate oxide transistors with higher voltages for peripheral circuits with a decoder circuit in between, it would have been obvious to one skilled in the art at

the time of the invention to construct other in between circuits for the purpose of creating a buffer between the low and high voltage regions of the circuit.

Response to Arguments

5. Applicant's arguments filed 04/29/99 have been fully considered but they are not persuasive.

In response to applicant's argument that Shimizu does not disclose the advantages of the present invention, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Applicant argues in regards to claims 1 and 2 that Shimizu fails to teach a "direct" connection between the transistor with not the thinnest gate insulation film and the Input/Output and Power Supply terminals. Examiner respectfully disagrees. The term, "directly" as stated by the applicant does not distinguish the claimed invention from the prior art. As interpreted by the office, "directly" is a connection through a transistor or through an interconnect (31) from one conducting location to another. If applicant wants to further distinguish the connection, he must

expound on the word "directly" to further distinguish the structure of the claimed invention from the prior art.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication from the examiner should be directed to Examiner Jesse A. Fenty at (703) 308-8137.

JAF

June 23, 1999

Mahshid Saadat

Mahshid Saadat
Supervisory Patent Examiner
Technology Center 2800